

Response to Double Patenting Rejections

Claims 1, 2, 6-8, 11, and 12 are provisionally rejected under 35 U.S.C. §101 as claiming the same invention as that of claims 1, 7, 11, and 12 of copending Application No. 09/715,253 (hereinafter referred to as “the ‘253 application”). Applicants respectfully traverse the foregoing double patenting rejections.

In this regard, it is asserted in M.P.E.P. §804(II)(A) that:

“In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. **“Same invention” means identical subject matter.** *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). ***Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist.*** (Emphasis added).

For at least the reasons set forth below, Applicants assert that, if the above test is properly applied in the instant case, it becomes readily apparent that claims 1, 2, 6-8, 11, and 12 of the instant application do not claim the same inventions as claims 1, 7, 11 and 12 of the ‘253 application.

Regarding claim 1 of the instant application, Applicants assert that this claim does not claim the same invention as claims 1, 7, 11, and 12 of the ‘253 application. In particular, claim 1 of the instant application recites features not recited in claims 1, 7, 11, and 12 of the ‘253 application, and it is, therefore, possible for an embodiment of a graphical display system to infringe claims 1, 7, 11, and 12 of the ‘253 application without infringing claim 1 of the instant application. For example, claim 1 of the instant application recites a “plurality of display devices.” However, claims 1, 7, 11, and 12 of the ‘253 application do not recite such a feature.

Thus, a graphical display system that employs less than two “display devices” may infringe claims 1, 7, 11, and 12 of the ‘253 application without infringing claim 1 of the instant application. Therefore, according to the test for statutory double patenting set forth in M.P.E.P. §804(II)(A), claim 1 of the instant application and claims 1, 7, 11, and 12 of the ‘253 application do not claim the “same invention,” and the provisional statutory double patenting rejection of claim 1 of the instant application is improper.

Similarly, each of the claims 2, 6-8, 11, and 12 of the instant application recites “a plurality of display devices” or “a plurality of display means,” and claims 1, 7, 11, and 12 of the ‘253 application recite no such features. Thus, for at least the reasons set forth above, Applicants assert that it is possible for an embodiment of a graphical display system to infringe claims 1, 7, 11, and 12 of the ‘253 application without infringing claims 2, 6-8, 11, and 12 of the instant application. Therefore, the provisional statutory double patenting rejections of claims 2, 6-8, 11, and 12 of the instant application are improper.

For at least the foregoing reasons, Applicants respectfully request that the provisional statutory double patenting rejections of claim 1, 2, 6-8, 11, and 12 of the instant application be withdrawn.

Furthermore, Applicants respectfully assert that a double patenting rejection based on the ‘253 application is improper until at least such application issues into a patent. Thus, Applicants request that the instant application be allowed to issue, notwithstanding the ‘253 application, once the instant application is otherwise within a condition for allowance pursuant to M.P.E.P. §822.01.

Response to §102(g) Rejections

In the Office Action, it is asserted that:

“Claims 1, 2, 6-8, 11-12 are directed to the same invention as that of claims 1, 7, 11 and 12 of commonly assigned Application No. 09/715253. The issue of priority under 35 U.S.C. 102 (g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.”

For at least the reasons set forth hereinabove in the arguments pertaining to the statutory double patenting rejections, Applicants respectfully traverse the above allegation that claims 1, 2, 6-8, 11, and 12 are directed to the same invention as claims 1, 7, 11, and 12 of the ‘253 application. Accordingly, it is not necessary for Applicants to state which entity is the prior inventor of the allegedly conflicting subject matter.

Response to §102(e) Rejections

Claims 1, 2, 6-8, 11, and 12 presently stand provisionally rejected under 35 U.S.C. §102(e) as allegedly anticipated by the ‘253 application. 35 U.S.C. §102(e) reads as follows:

“(e) the invention was described in—

(1) an application for patent, published under section 122(b), by another ***filed in the United States before the invention by the applicant for patent***, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another ***filed in the United States before the invention by the applicant for patent***, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351 (a)” (Emphasis added).

Thus, for a patent application or a patent to be a valid prior art reference under 35 U.S.C. §102(e), the patent application or patent must at least be “filed before” the instant application. Applicants respectfully assert that the ‘253 application and the instant application were filed on the same day. Thus, the ‘253 application was not “filed before” the instant application and, therefore, may not be used to reject the claims of the instant application under 35 U.S.C. §102(e).

For at least the foregoing reasons, Applicants respectfully assert that the provisional rejections of claim 1, 2, 6-8, 11, and 12 under 35 U.S.C. §102(e) are improper and request that these rejections be withdrawn.

Response to §103 Rejections

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, e.g., *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981). Furthermore, “35 U.S.C. §103 requires that obviousness be determined with respect to the invention as a whole. This is essential for combination inventions, for generally all combinations are of known elements.” *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543 (Fed. Cir. 1985)(citations omitted).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §103 as purportedly being obvious to *MacInnis* (U.S. Patent No. 6,501,480) in view of *Computer Wall II*, RGB Spectrum, Inc. Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000,

<http://www.rgb.com/Webpages/prodpgs/cwall.html> (hereinafter referred to as "*Computer Wall*

II"). Claim 1, as amended, reads as follows:

1. A single logical screen (SLS) graphical display system, comprising:
an interface configured to receive graphical data defining an image;
a plurality of display devices; and
a plurality of graphical acceleration units, each of said plurality of graphical acceleration units respectively interfaced with one of said plurality of display devices and configured to render a portion of said graphical data to said one display device such that said display devices display said image as a single logical screen, wherein ***at least one of said graphical acceleration units comprises:***
a first graphical pipeline configured to render graphical data;
a second graphical pipeline configured to render graphical data;
and
a compositor configured to interface with said one display said graphical data rendered by said first and second graphical pipelines.
(Emphasis added).

Applicants respectfully assert that the alleged combination of *MacInnis* and *Computer Wall II* fails to suggest or teach at least the features of pending claim 1 highlighted hereinabove.

In this regard, *MacInnis* appears to describe an integrated circuit that is capable of receiving one or more video input signals and then producing a video output signal based on the one or more video input signals. See FIG. 1 and column 3, lines 30-38. Indeed, in one embodiment, it appears that the video output signal may comprise video data from a video input stream 12 and graphics data from a CPU 22. In such an embodiment, the alleged "compositor" 60 apparently blends the data from the video input stream 12 with the graphics data from the CPU 22. See column 5, lines 38-41.

Further, the integrated circuit of *MacInnis* appears to include an "accelerator" 64 for rendering the graphics data from the CPU 22. However, there is no such "accelerator" for the video input stream 12. To the contrary, *MacInnis* appears to suggest that the input video stream 12 may correspond to a television signal and that the integrated circuit may combine such a video signal with the graphics data rendered by the "accelerator" 64 thereby including graphical

images with the television (*i.e.*, “video”) images defined by the input data stream 12. See column 1, lines 45-48. Thus, when the cited art and, in particular, *MacInnis* is properly considered “as a whole,” as required by *Interconnect Planning*, it becomes readily apparent that there is no motivation or reason provided in the cited art to include, within the integrated circuit of *MacInnis*, a “graphical pipeline” for the input data stream 12. As such, the alleged combination of *MacInnis* and *Computer Wall II* fails to suggest at least a second “graphical pipeline” within an alleged “graphical acceleration unit.” Thus, the alleged combination fails to suggest at least the combination of features of claim 1 highlighted hereinabove.

For at least the foregoing reasons, Applicants submit that the cited art fails to suggest or teach each feature of claim 1. Accordingly, the rejection of pending claim 1 under 35 U.S.C. §103 is improper and should be withdrawn.

Claims 2-6 and 15-17

Claims 2-6 presently stand rejected in the Office Action under 35 U.S.C. §102(a) as allegedly anticipated by *MacInnis*. Furthermore, claims 15-17 have been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 2-6 and 15-17 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2-6 and 15-17 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §103 as allegedly unpatentable over *MacInnis* in view of *Computer Wall II*. Claim 7, as amended, reads as follows:

7. A single logical screen (SLS) graphical display system, comprising:
means for receiving a graphical command;
first rendering means for rendering a first portion of graphical data included within said graphical command, ***said first rendering means including a plurality of pipeline means for rendering said first graphical data portion in parallel and a compositing means for compositing said first rendered portion;***
second rendering means for rendering a second portion of said graphical data, ***said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion;***
first display means for displaying a first image based on said first composited portion; and
second display means for displaying a second image based on said second composited portion,
wherein said first and second images define at least a portion of a single logical screen image. (Emphasis added).

For at least the reasons set forth hereinabove in the arguments for allowance of claim 1, Applicants submit that the alleged combination fails to disclose at least the features of claim 7 highlighted hereinabove. Thus, the rejection of claim 7 under 35 U.S.C. §103 is improper and should be withdrawn.

Claims 8-10

Claims 8-10 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly unpatentable over *MacInnis* in view of *Computer Wall II*. Applicants submit that the pending dependent claims 8-10 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8-10 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 11

Claim 11 presently stands rejected under 35 U.S.C. §103 as allegedly unpatentable over *MacInnis* in view of *Computer Wall II*. Claim 11, as amended, reads as follows:

11. A single logical screen (SLS) graphical display method, comprising:
receiving graphical data defining an image;
rendering different portions of said graphical data via different ones of a plurality of graphical acceleration units;
in at least one of said graphical acceleration units, compositing the graphical data rendered by said at least one graphical acceleration unit; and
displaying said image across a plurality of display devices as a single logical screen, said displayed image based on said composited graphical data,
wherein said rendering comprises rendering, in said at least one graphical acceleration unit, a respective one of said graphical data portions via each of a plurality of pipelines. (Emphasis added).

For at least the reasons set forth hereinabove in the arguments for allowance of claim 1, Applicants submit that the alleged combination fails to disclose at least the features of claim 11 highlighted hereinabove. Thus, the rejection of claim 11 under 35 U.S.C. §103 is improper and should be withdrawn.

Claims 12-14 and 18-20

Claims 12-14 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly unpatentable over *MacInnis* in view of *Computer Wall II*. Furthermore, claims 18-20 have been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 12-14 and 18-20 contain all features of their respective independent claim 11. Since claim 11 should be allowed, as argued hereinabove, pending dependent claims 12-14 and 18-20 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 21

Claim 21 has been newly added via the amendments set forth herein. Claim 21 presently reads as follows:

21. A single logical screen (SLS) graphical display system, comprising:
an interface configured to receive a graphical command;
a plurality of display devices; and
a plurality of graphical acceleration units, each of said graphical acceleration units respectively interfaced with a respective one of said plurality of display devices and configured to render, in parallel, a different portion of graphical data included in said graphical command, each of said graphical acceleration units comprising a compositor configured to composite said graphical data portion rendered by said each graphical acceleration unit.

Applicants respectfully assert that the cited art fails to disclose or suggest each of the features of claim 21 set forth above. Accordingly, Applicants submit that claim 21 is allowable.

Claims 22-24

Claims 22-24 have been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 22-24 contain all features of their respective independent claim 21. Since claim 21 should be allowed, as argued hereinabove, pending dependent claims 22-24 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 25

Claim 25 has been newly added via the amendments set forth herein. Claim 25 presently reads as follows:

25. A single logical screen (SLS) graphical display method, comprising:
receiving a graphical command;
displaying at least a portion of a single logical screen image via a
plurality of display devices; and
for each of said display devices, rendering in parallel a different portion
of graphical data included in said graphical command and compositing said
rendered portion.

Applicants respectfully assert that the cited art fails to disclose or suggest each of the features of
claim 25 set forth above. Accordingly, Applicants submit that claim 25 is allowable.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be
withdrawn and that this application and all presently pending claims be allowed to issue. If the
Examiner has any questions or comments regarding Applicants' response, the Examiner is
encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted ,

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**

By:



Jon E. Holland

Reg. No. 41,077

(256) 704-3900 Ext. 103

Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

ANNOTATED VERSION OF MODIFIED CLAIMS

TO SHOW CHANGES MADE

The following is a marked up version of the amended claims, wherein brackets denote deletions and underlining denotes additions.

1. (Once Amended) A single logical screen (SLS) graphical display system, comprising:
 - an interface configured to receive graphical data defining an image;
 - a plurality of display devices; and
 - a plurality of graphical acceleration units, each of said plurality of graphical acceleration units respectively interfaced with one of said plurality of display devices and configured to render a portion of said graphical data to said one display device such that said display devices display said image as a single logical screen, wherein at least one of said graphical acceleration units comprises:
 - a first graphical pipeline configured to render graphical data [from said portion rendered by said at least one graphical acceleration unit];
 - a second graphical pipeline configured to render graphical data [from said portion rendered by said at least one graphical acceleration unit]; and
 - a compositor configured to interface with said one display said graphical data rendered by said first and second graphical pipelines.

φ 12. (Once Amended) A single logical screen (SLS) graphical display system,
comprising:

means for receiving a graphical command;

first rendering means for rendering a first portion of graphical data included within said graphical command [to a plurality of frame buffers], said first rendering means including a plurality of pipeline means for rendering [a] said first graphical data portion [of said graphical data to one of said frame buffers] in parallel and a compositing means for compositing said first rendered portion;

second rendering means for rendering a second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion; [and]

[a plurality of] first display means[, each of said display means] for displaying [an] a first image based on said first composited portion; and [graphical data stored in a respective one of said plurality of frame buffers]

second display means for displaying a second image based on said second composited portion,

wherein said first and second images define at least a portion of a single logical screen image.

8. (Once Amended) The system of claim 7, wherein each of said plurality of pipeline means of said first rendering means includes a means for mathematically combining a different offset to coordinate values included in said first graphical data portion [of said graphical data], and wherein said compositing means of said first rendering means includes a means for blending color values associated with corresponding coordinate values within said first graphical data portion [of said graphical data].

9. (Once Amended) The system of claim 7, wherein said first rendering means includes a means for receiving an input identifying a coordinate range, and wherein one of said plurality of pipeline means of said first rendering means includes a means for discarding graphical data from said first graphical data portion based on said coordinate range.

10. (Once Amended) The system of claim 9, wherein each of said plurality of pipeline means of said first rendering means is configured to super sample graphical data from said first graphical data portion, and wherein said compositing means of said first rendering means includes a means for blending color values included in said super sampled graphical data.

11. (Once Amended) A single logical screen (SLS) graphical display method, comprising [the steps of]:

[providing a plurality of graphical acceleration units, at least one of said graphical acceleration units including a plurality of graphical pipelines;

providing a plurality of display devices;]

receiving graphical data defining an image;

rendering different portions of said graphical data via different ones of a plurality of [said] graphical acceleration units; [and]

in at least one of said graphical acceleration units, compositing the graphical data rendered by said at least one graphical acceleration unit; and

displaying said image across [said] a plurality of display devices as a single logical screen, said displayed image based on said composited graphical data [rendered in said rendering step],

wherein said rendering [step includes the step of] comprises rendering, in said at least one graphical acceleration unit, a respective one of said graphical data portions [graphical data from one of said portions] via each of [said] a plurality of pipelines.

12. (Once Amended) The method of claim 11, wherein said rendering [step] further [includes the steps of:] comprises mathematically combining different offsets with coordinate values included in one of said graphical data portions, and wherein said compositing comprises [rendered via said plurality of pipelines; and] blending color values associated with [corresponding] said coordinate values [included in said graphical data rendered via said plurality of pipelines].

13. (Once Amended) The method of claim 11, further comprising [the steps of]:
receiving an input identifying a coordinate range; and
discarding, via one of said plurality of graphical pipelines, graphical data from [said] one
of said portions based on said coordinate range.

14. (Once Amended) The method of claim 13, wherein said rendering [step includes
the steps of:] further comprises super-sampling graphical data from [said] one of said portions,
[via said plurality of pipelines;] and wherein said compositing further comprises blending color
values included in said super sampled graphical data.